Technical University of Denmark

Popular science summary of the PhD thesis

PhD student	Jens Christian Hertel
Title of the PhD thesis	High Efficiency Synchronous Rectifier using Phase Locked Loops
PhD school/Department	Department of Electrical Engineering - Electronics

Science summary

* Please give a short popular summary in Danish or English (approximately half a page) suited for the publication of the title, main content, results and innovations of the PhD thesis also including prospective utilizations hereof. The summary should be written for the general public interested in science and technology:

This thesis expands the knowledge needed for miniaturization of power converters, through increasing the switching frequencies of Switch Mode Power Supplies (SMPS). One of the crucial elements of the current topologies of SMPS is the rectifier. Most commonly the rectifier in higher frequency (MHz) SMPS is implemented using the passive diode, out of both simplicity and lack of other solutions. However, the diode is inherently very lossy, and sets a limit on how small higher frequency SMPS can be.
In this thesis two new circuit methods are utilized to implement a rectifier with transistors instead of diodes. By switching the transistor at specific times, the power losses can be minimized significantly. The two circuit methods presented in this thesis are the phase locked loop and the delay locked loop.
The phase locked loop works by tuning the phase and frequency of an oscillator to an incoming signal. Similarly, the delay locked loop can synchronize the phases of two signals by adjusting a delay element. These two methods allow rectifiers to operate at much higher frequencies, because otherwise critical delays of gate drivers and level shifters can be included inside the loop allowing for accurate switching of the transistors for loss-minimization.
The proposed methods have been implemented in two integrated circuits, and two prototype rectifiers are designed around them. It is shown that integrated circuits can increase the efficiency of the power supplies by up to 2 percent point, and in the implemented prototype reduce the volume needed by 11%.
These circuits are fully monolithically integrable on CMOS integrated circuits and can easily operate at higher frequencies, paving the path for even smaller power supplies.

Please email the summary to the PhD secretary at the department